JAPAN PATENT OFFICE

PATENT LAID-OPEN OFFICIAL GAZETTE

Laid-Open No.
H.5-13664

Laid-Open
H.5 (1993) Jan. 22

Application No.: H.3-185625

Filed: H.3 (1991) June 29

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(54) [TITLE OF THE INVENTION]
Semiconductor Device

(57) [ABSTRACT]
[Objective]
To process resin-sealed semiconductor devices into a multi-chip structure that has good qualities for mass-production.

[Configuration]
Multiple semiconductor chips are attached to one side of TAB tape along the length of the TAB tape. The TAB tape is double-folded to create a three-dimensional arrangement of semiconductor chips, which is then sealed in resin.

[WHAT IS CLAIMED]
[Claim 1]
A semiconductor device characterized in that;
on one side of a piece of TAB tape, leads are connected to the electrodes of multiple semiconductor chips which are arranged along the length of the TAB tape;
the above TAB tape is double-folded so that the above semiconductor chips are positioned above a single region to create a three-dimensional placement of the semiconductor chips; and the chips are then sealed while in this state.

[DETAILED DESCRIPTION OF THE INVENTION]
[0001]
[Scope of Utilization in Industry]
This invention relates to semiconductor devices, and in particular to an effective technology that is suitable for a semiconductor device which is a resin-sealed set of multiple semiconductor chips.

[0002]

[Prior Art]

In general, a resin-sealed semiconductor device is made up of a single resin-sealed semiconductor chip. Semiconductor control devices and semiconductor storage devices that have a single resin-sealed semiconductor chip have been placed in two-dimensional arrangements and mounted on multi-layered circuit boards called mother-boards.

[0003]

[Problem to be Solved by the Invention]

However, with the conventional technique described above, the wiring from the resin-sealed semiconductor devices occupies a greater proportion of the area of the multi-layered circuit board as the number of bits handled by the data bus increases. As the density of the wiring pattern increases, the wiring films become finer and longer. In addition, the sizes of resin-sealed semiconductor devices increase as they are provided with more and more pins, and this makes for a larger overall size of the resin-sealed semiconductor devices when they are mounted on a multi-layered circuit board.

[0004]

This invention is intended to solve the problem described above by providing a technique that allows easier manufacturing of multi-chip semiconductor devices.

[0005]

[Means for Solving the Problem]

The semiconductor device of this invention is characterized by the attachment of multiple semiconductor chips on one side of a strip of TAB tape along the length of the TAB tape, and the double-folding of the TAB tape to create a resin-sealed three-dimensional placement of the semiconductor chips.

[0006]

[Embodiment]

The semiconductor device of this invention is described in detail below, on the basis of an embodiment shown in the accompanying drawings. Figure 1, (A) and (B), shows an example of an embodiment of the semiconductor device of this invention: (A) is the cross-sectional view and (B) is the cross-sectional view of the TAB tape before it is double-folded; figure 2 is the wiring diagram that shows the connection between the electrodes of the semiconductor chips and the leads of the TAB tape; and figure 4 is the plan view of the lead frame on which the outer leads that bring out the semiconductor device's electrodes are formed.

[0007]

To begin with, an outline of the configuration of the semiconductor device is given below, with reference to figure 1 (A). Item 1 is the TAB tape. This extends over base film 2 of, for example, polyimide, and on which leads 3 of, for example, Cu foil, are formed to bring out the electrodes (hereinafter referred to as "TAB leads"). The specific form of this will later be described in detail with reference to figure 1 (B).

[0008]

Items 4a and 4b are semiconductor chips and their electrodes 5, 5, ... are connected to TAB leads 3, 3,... on TAB tape 1 via bumps 6, 6, ... , which are made of, for example, Au. Said semiconductor chips 4a and 4b are placed on one side of TAB tape 1 (for example, the side on which TAB leads 3 are formed) along the direction of its length. TAB tape 1 is double-folded so that the part to which semiconductor chip 4a is connected lays on the part to which semiconductor chip 4b is connected and so that semiconductor chips 4a and 4b are positioned back to back.

[0009]

The back sides of said semiconductor chips 4a and 4b are bonded together via die pad 7 on the lead frame, which will be described later. Items 12 and 12 are the adhesive, which is, for example, epoxy resin, that bonds semiconductor chips 4a and 4b to die pad 7. Items 8, 8, … are the leads of the lead frame, each of which is connected with one end of a TAB lead 3, 3, … (the end on the 4b side of the TAB tape). Item 9 is the sealing resin.

[0010]

Next, the form of TAB tape 1 is described below, with reference to figure 1 (B). All of the TAB leads 3, 3, … are formed such that they run parallel to each other along the length of TAB tape 1. TAB tape 1 is for a single semiconductor device (which contains two semiconductor chips), and a series of many such blocks extends in the direction of its length. Each block may be divided into chip bonding section 1, to which semiconductor chip 4a is bonded; a section bar; chip bonding section 2, to which semiconductor chip 4b is bonded; a section bar; and an outer lead section.

[0011]

On each of semiconductor chips 4a and 4b, electrodes 5, 5, … are placed along the long sides of the chip's perimeter. Electrodes 5a, 5a,… are placed with a constant pitch along one long side of semiconductor chips 4a and 4b, and electrodes 5b, 5b, … are placed, with the same pitch, along the other long side of semiconductor chips 4a and 4b. However, the positions of electrodes 5a, 5a, … on one long side and electrodes 5b on the other long side are positioned shifted by 1/2 pitch, so the lines that connect the individual electrodes 5a, 5b, 5b,… of one semiconductor chip 4 form a zigzag pattern.

[0012]

Electrodes 5a and 5a of two semiconductor chips 4a and 4b are connected to 3a of TAB leads 3, and electrodes 5b

and 5b are connected to 3b of TAB leads 3. TAB leads 3a and 3b are distributed in an alternating pattern, and electrodes 5a and 5b of semiconductor chips 4a and 4b are connected to their corresponding counterparts by the respective TAB leads 3a and 3b. At the same time, electrodes 5a and 5b of semiconductor chips 4a and 4b are electrically brought out of resin 9 via TAB leads 3a and 3b and lead 8 of the lead frame.

[0013]

Power-supply-potential electrode 5d and ground-potential electrode s of semiconductor chips 4a and 4b are placed as exceptions, with half the pitch of electrodes 5a, 5a, … at the end of the chip's long side where electrodes 5a, 5a, … are placed, and are connected with TAB leads 3d and 3s of TAB tape 1, respectively.

[0014]

Items 2a, 2a, … are support bars that support the inner lead section of base film 2, and item 2b is a section bar that is placed in the space between semiconductor chips 4a and 4b. Two slits for folding (slit 10) are formed on section bar 2b, and allow TAB tape 1 to be double-folded at section bar 2b.

[0015]

Item 11 is the lead frame (see figure 3), and the two-dot-broken line shows the position of sealing resin 9. By double-folding TAB tape 1, each back side of semiconductor chips 4a and 4b, which are connected to one side of TAB tape 1, is bonded to one side of die pad 7 of this lead frame 11 via adhesive 12 and 12, and the outer lead section of TAB tape 1 is connected to leads 8, 8, … of lead frame 1.

[0016]

With a semiconductor device like this, since the two semiconductor chips 4a and 4b are placed on the either

side of die pad 7 and are sealed in resin, a multi-chip device is created without increasing the area occupied by the device. This makes an increase in the density of circuit integration within the device possible. The electrical connection between semiconductor chips 4a and 4b of the resin-sealed semiconductor device is made in sealing resin 9. This eliminates the need to provide wiring, in order to make said electrical connection, on the multi-layered circuit board on which the resin-sealed semiconductor device is mounted. Accordingly, higher-capacity circuitry can be mounted without increasing the number of wires, the length of the wiring, or the density of the wiring.

[0017]

In addition, with this semiconductor device, qualities in terms of mass-production are improved and assembly is facilitated because the device can be manufactured by a method in which multiple semiconductor chips 4a, 4b, … are connected to a long strip of TAB leads 1, and TAB tape 1 is then cut to divide it up into individual blocks (see figure 1 (B)) and presented for the step of bonding semiconductor chips 4a and 4b onto die pad 7.

[0018]

Then, each block of TAB tape 1, 1, … is double-folded to bond semiconductor chips 4a and 4b to die pad 7. It will then be possible to seal this in resin in a state such that the TAB leads are connected to the inner lead section of leads 8, 8,… on lead frame 11. At the time of resin injection, each of semiconductor chips 4a and 4b is fixed on one side of die pad 7. As a result of this and of the injected resin, there is little risk of misalignment of semiconductor chips 4a and 4b, and the occurrence of defects becomes more difficult. The manufacture of multi-chip devices is therefore made easier.

[0019]

Figure 4 is a cross-sectional view that shows a different embodiment of the semiconductor device of this invention. In this embodiment, resin sealing is not provided by transfer molding but is provided in the following steps: after connecting semiconductor chips 4a and 4b to TAB tape 1, connecting semiconductor chips 4a and 4b to die pad 13, and cutting off the unnecessary parts of TAB tape 1, the outer lead sections of TAB leads 3, 3, … are connected to wiring film 15, 15, … on the surface of circuit board 14; semiconductor chips 4a and 4b are then sealed in resin 16 by potting. A eutectic alloy of Au and Sn, for example, is used to make the connections between the outer-lead sections of TAB leads 3, 3, … and wiring film 15, 15, … on circuit board 14. In this embodiment, die pad 13 may either have an insulating characteristic or may be made of metal for improved radiation.

[0020]

Figure 5 is a cross-sectional view that shows another different embodiment of the semiconductor device of this invention. In this embodiment, by increasing the number of double-folds, two pairs of semiconductor chips 4a and 4b, which are connected back to back via die pad 13, are arranged in an ascending three-dimensional way in a single region. This can provide a circuit-integration density which is double that of the embodiments in figure 1 and figure 4.

[0021]

In this embodiment, TAB leads are connected to wiring film 15 on the circuit board 14 and the sealing in resin 16 takes place as potting. However, the technique of this embodiment for increasing the number of pairs of semiconductor chips 4a and 4b by increasing the number of double-folds is also applicable to semiconductor devices of the transfer-molded type.

[0022]

Moreover, in this embodiment, and in connection with the increased number of double-folds in the TAB tape, TAB leads 3, 3, … are folded in layers in the section between the pair of semiconductor chips 4a and 4b on the lower side of TAB tape 1 and the pair on the upper side of TAB tape 1. Accordingly, lowered impedance can be expected in the transmission routes for signals and the power supply.

[0023]

However, on the other hand, there is a risk of a minor twist causing a short-circuit failure. An insulating film may be inserted in the folded section to avoid such short-circuit failures. Another way to prevent short-circuit failures is to coat the TAB tape's leads with an insulating film such as a film of solder resist. As has been described above, there are various possible ways of embodying the semiconductor device of this invention.

[0024]

[Advantages of the Invention]

A semiconductor device of this invention is characterized in that;
on one side of a piece of TAB tape, leads are connected to the electrodes of multiple semiconductor chips which are arranged along the length of the TAB tape;
the above TAB tape is double-folded so that the above semiconductor chips are positioned above the area in which they are placed, to create a three-dimensional placement of the semiconductor chips; and the chips are then sealed while in this state. Accordingly, the semiconductor device of this invention makes it possible to create a multi-chip device with an increased density of circuit integration but no increase in the area the device occupies. The electrical connection between semiconductor chips in the resin-sealed semiconductor device is made within the device, so it is not required to be made on the multi-layered circuit board on which the resin-sealed semiconductor device is mounted. Accordingly, higher-capacity circuitry can be mounted without increasing the

number of wiring lines, the length of the wiring, or the density of wiring.

[0025]

In addition, with this semiconductor device, qualities in terms of mass-production are improved and assembly is facilitated because the device can be manufactured by a method in which multiple semiconductor chips are connected to a long strip of TAB leads, and the TAB tape is then cut to divide it up into individual blocks and then presented for the step of bonding semiconductor chips onto the die pad. Furthermore, each block of the TAB tape is double-folded to bond the semiconductor chips onto the die pad. It will then be possible to seal this in a state such that the TAB leads are connected to the inner lead section of the leads on the lead frame. When sealed in resin in such a way, a semiconductor chip is affixed to each side of the die pad at the time of resin injection. As a result of this and of the injected resin, there is little risk of misalignment of semiconductor chips, and the occurrence of defects becomes more difficult. The manufacture of multi-chip devices is therefore made easier.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Figure 1]

Figure 1, (A) and (B), shows an example of an embodiment of the semiconductor device of this invention. (A) is a cross-sectional view, and (B) is a plan view of the TAB tape.

[Figure 2]

Figure 2 is a wiring diagram for the above embodiment, which shows the connection between the semiconductor chips' electrodes and the TAB tape.

[Figure 3]

Figure 3 is a plan view of the lead frame used in the above embodiment.

[Figure 4]

Figure 4 is a cross-sectional view of a semiconductor device, which is a different embodiment of this invention.

[Figure 5]

Figure 5 is a cross-sectional view of a semiconductor device, which is another different embodiment of this invention.

[Description of Symbols]

1: TAB tape
3(3a, 3b, 3c, 3d): TAB leads
4a, 4b: Semiconductor chips
5: Electrode
7: Die pad
9: Resin
13: Die pad

Embodiment

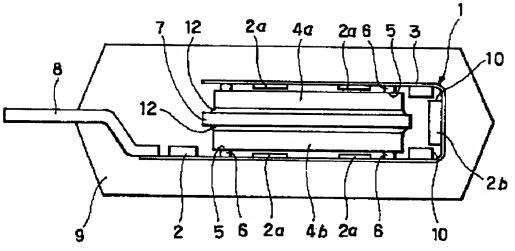
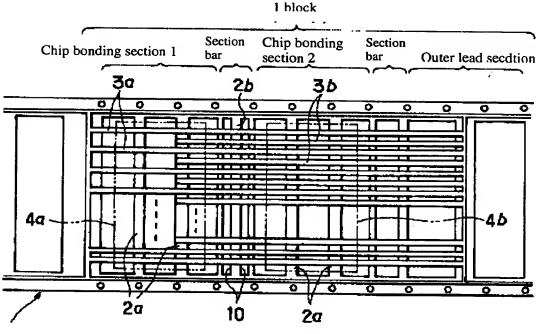
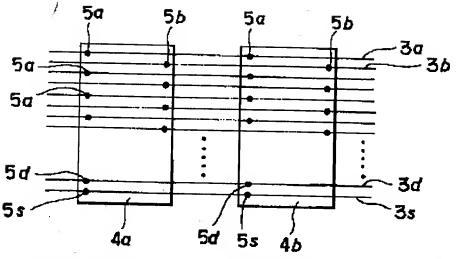


Figure 1 (A) Cross-sectional View



1: TAB tape
3 (3a, 3b) ...: TAB lead
4a, 4b: Semiconductor chip
5: Electrode
7: Die pad
9: Resin

Figure 1 (B) Plan View of TAB Leads



3 (3a, 3b) : TAB lead
4 (4a, 4b) : Semiconductor chip
5 (5a, 5b) : Electrode
7: Die pad

Figure 2 Wiring Diagram of Connection between Chips' Electrodes and TAB Leads

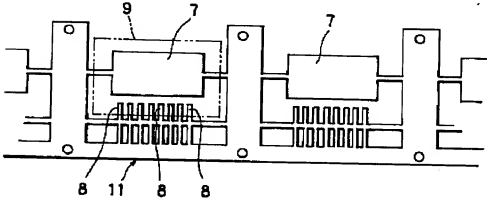
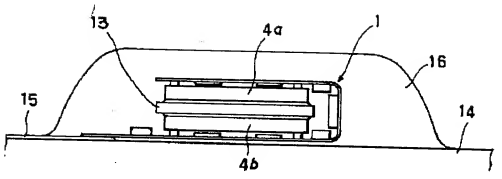


Figure 3 Plan View of Lead Frame



1: TAB tape
4a, 4b : Semiconductor chip
13: Die pad
16: Resin

Figure 4 Cross-sectional View of a Different Embodiment

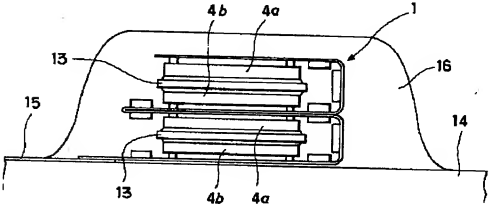


Figure 5 Cross-sectional View of Another Different Embodiment

Amendment of Proceedings (Voluntary)

H.3 (1991) Nov. 21

To: Commissioner of the Patent Office

1. Designation of the case
   Application No.: H.3-185625

2. Title of the invention
   Semiconductor device

3. Person who amends
   Relation with the case: Applicant for patent
   Sony Corporation
   6-7-35 Kita-shinagawa,
   Shinagawa-ku, Tokyo

4. Attorneys, Agents
   Sony Corporation
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   Shinagawa-ku, Tokyo

   Patent attorney: Hideaki Ogawa

5. Parts to be amended
   Embodiment: [0006]
   Advantages of the Invention: [0024]

6. Contents of the amendment
   Refer to the following passages.

Revised part is underlined.

[0006]
[Embodiment]

The semiconductor device of this invention is described in detail below, on the basis of an embodiment shown in the accompanying drawings. Figure 1, (A) and (B), shows an example of an embodiment of the semiconductor device of this invention: (A) is the cross-sectional view and (B) is the plan view of the TAB tape before it is double-folded; figure 2 is the wiring diagram that shows the connection between the electrodes of the semiconductor chips and the leads of the TAB tape; and figure 3 is the plan view of the lead frame on which the outer leads that bring out the semiconductor device's electrodes are formed.

[0024]

[Advantages of the Invention]

A semiconductor device of this invention is characterized in that;
on one side of a piece of TAB tape, leads are connected to the electrodes of multiple semiconductor chips which are arranged along the length of the TAB tape;
the above TAB tape is double-folded so that the above semiconductor chips are positioned above the area in which they are placed, to create a three-dimensional placement of the semiconductor chips; and the chips are then sealed while in this state. Accordingly, the semiconductor device of this invention makes it possible to create a multi-chip device with an increased density of circuit integration but no increase in the area the device occupies. The electrical connection between semiconductor chips in the resin-sealed semiconductor device is made within the device, so it is not required to be made on the multi-layered circuit board on which the resin-sealed semiconductor device is mounted. Accordingly, higher-capacity circuitry can be mounted without increasing the number of wiring lines, the length of the wiring, or the density of wiring.

(Note: "Johoni" in Japanese has been revised to "Johono." No amendments in English version.)